address electrodes in respective arrays of X and Y dimension address electrodes in an ac plasma panel, said addressing apparatus comprising:

means for applying a high level pulse of one polarity to [an]a ~~polarity of~~ plurality address electrodes of one dimension array;

means for [selecting whether to]selective discharging of non-selected address electrodes of said plurality and maintaining the high level of one polarity at [said]selected address electrodes of said plurality [or to bring the electrode to a low level of said one polarity]in accordance with desired information to be entered into the plasma panel; and

means for applying a high level pulse of opposite polarity to a respective address electrode of the other dimension array after said selective discharging of non-selected address electrodes[a high level of one polarity has been selected at said address electrode of said one dimension array,] for discharging [the defined address]cells at said selected address electrodes and entering the desired information into the plasma panel.--

--~~17~~ 2. (Amended) Addressing apparatus according to claim ~~16~~ 1, including means for applying a second high level pulse of said one polarity to said plurality of address electrodes of said one dimension array after the end of said high level pulse of opposite polarity for enabling the controllable discharging of said selected address electrodes from said high level to said low level of said one polarity.--

--~~18~~ 3. (Amended) Addressing apparatus for addressing [at least one]cells defined by the intersection of respective address electrodes in respective arrays of X and Y dimension address electrodes in an ac plasma panel, said addressing apparatus comprising:

means for charging [an]a plurality of address electrodes of one dimension array to a high level of one polarity;

means for [selecting whether to]selective discharging of non-selected charged address electrodes of said plurality and maintaining the high level of one polarity at [said]selected charged address electrodes [or to bring the electrode to a low level of said one polarity]in accordance with desired information to be entered into the plasma panel; and

means for applying a high level of opposite polarity charge to a respective address electrode of the other dimension array after said selective discharging of non-selected charged address electrodes[a high level of one polarity has been selected at said address electrode of said one dimension array,] for discharging [the defined address]cells at said selected charged address electrodes and entering the desired information into the plasma panel.--

--~~19~~ 4. (Amended) Addressing apparatus according to claim ~~18~~ 3, wherein said means for charging [the]said plurality of address electrode of one dimension array includes means for applying a high level pulse of said one polarity to said plurality of address electrodes.--

--~~20~~ 5. (Amended) Addressing apparatus according to claim ~~18~~ 3, including means for applying a high level pulse of said one polarity to said plurality of address electrodes of one dimension array after entering said desired information into the plasma panel for enabling the controllable discharging of said selected charged address electrodes from said high level to said low level of said one polarity.--

6

--~~21~~. (Amended) Addressing apparatus according to claim 5 ~~20~~, wherein said means for charging [the]said plurality of address electrodes of one dimension array includes means for applying a high level pulse of said one polarity to said plurality of address electrodes.

7

--~~22~~. (Amended) A method of addressing [at least one]address cells defined by the intersection of respective address electrodes in respective arrays of X and Y dimension address electrodes in an ac plasma panel, said method of addressing comprising the steps of:

cont. charging [an]a plurality of address electrodes of one dimension array to a high level of one polarity;

C1 selective discharging of non-selected charged address electrodes of said plurality without discharging selected charged address electrodes of said plurality[selecting whether to maintain the charged electrode at the high level or to bring the electrode to a low level of said one polarity] in accordance with desired information to be entered into the plasma panel; and

applying a high level of opposite polarity charge to a respective address electrode of the other dimension array for discharging [the defined]address cells [where]associated with the selected charged address electrodes of said plurality [is maintained at the high level]and entering the desired information into the plasma panel.--

8 7

--~~23~~. (Amended) The method of claim ~~22~~, wherein said charging includes applying a high level pulse of said one polarity to said plurality of address electrodes of one dimension array.--

9 7

--24. (Amended) The method of claim 22, including the further step of applying a high level pulse of said one polarity to said plurality of address electrodes of one dimension array after entering said desired information into the plasma panel for enabling the controllable discharging of said selected charged address electrodes[from said high level to said low level of said one polarity].--

10 9

--25. (Amended) The method of claim 24, wherein said charging includes applying a first high level pulse of said one polarity to said plurality of address electrodes of one dimension array.--

Cont.

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C1

--26. (Amended) Addressing apparatus for addressing [at least one]pixels defined by the intersection of respective address electrodes in respective arrays of X and Y dimension address electrodes in a display panel, said addressing apparatus comprising:

[(a)] means for applying a high level pulse of one polarity to [an]address electrodes of one dimension array;

[(b)] means for selective discharging of non-selected address electrodes without discharging selected address electrodes[selecting whether to maintain the high level of one polarity at said address electrode or to bring the electrode to a low level of said one polarity] in accordance with desired information to be entered into the display panel; and

[(c)] means for applying a high level pulse of opposite polarity to a respective address electrode of the other dimension array after said selective discharging[a high level of one polarity has been selected at said address electrode of said one

dimension array] for entering the desired information into the display panel.--

12
--~~27~~. (~~Amended~~) Addressing apparatus according to claim 11 ~~26~~, including means for applying a second high level pulse of said one polarity to said address electrodes of said one dimension array after the end of said high level pulse of opposite polarity for enabling the controllable discharging of said selected address electrodes[from said high level to said low level of said one polarity].--

13
--~~28~~. (~~Amended~~) Addressing apparatus for addressing [at least one]pixels defined by the intersection of respective address electrodes in respective arrays of X and Y dimension address electrodes in a display panel, said addressing apparatus comprising:

Cont.
C1

means for charging [an]address electrodes of one dimension array to a high level of one polarity;

means for [selecting whether]selective discharging of non-selected charged address electrodes without discharging selected charged address electrodes to maintain the high level of one polarity at said selected charged address electrodes [or to bring the electrode to a low level of said one polarity]in accordance with desired information to be entered into the display panel; and

means for applying a high level of opposite polarity charge to a respective address electrode of the other dimension array after said selective discharging of non-selected charged address electrodes[a high level of one polarity has been selected at said address electrode of said one dimension array] for entering the desired information into the display panel.--

14

--~~29~~. (Amended) Addressing apparatus according to claim 13 ~~28~~, including means for applying a high level pulse of said one polarity to said address electrodes of one dimension array after entering said desired information into the display panel for enabling the controllable discharging of said selected charged address electrodes from said high level to [said]a low level of said one polarity.--

15

--~~30~~. (Amended) A method of addressing [at least one]address cells defined by the intersection of respective address electrodes in respective arrays of X and Y dimension address electrodes in a display panel, said method of addressing comprising the steps of:

Cont.

C1

[a] charging [an]address electrodes of one dimension array to a high level of one polarity;

[b] [selecting whether to maintain the charged electrode at the high level or to bring the electrode to a low level of said one polarity]selective discharging non-selected but not selected charged address electrodes in accordance with desired information to be entered into the display panel; and

[c] applying a high level of opposite polarity charge to a respective address electrode of the other dimension array after said selective discharging for entering the desired information into the display panel.--

16 15

--~~31~~. (Amended) The method of claim ~~30~~, including the further step of applying a high level pulse of said one polarity to said address electrode of one dimension array after entering said desired information into the display panel for enabling the controllable discharging of said selected charged address

electrodes[from said high level to said low level of said one polarity].

17

--32. (Amended) A display panel comprising:

an array of X dimension address electrodes;

an intersecting array of Y dimension address electrodes, where intersections between respective X and Y address electrodes define respective display pixels;

address means for applying an addressing signal during an addressing cycle to selected X and Y address electrodes to activate at least one display pixel;

said address means including, means for charging [an]more than one address electrode of [one]said X or Y dimension array to a high level of one polarity;

cont. C1

means for [selecting whether to maintain the high level of one polarity at said address electrode or to bring the electrode to a low level of said one polarity]selective discharging non-selected but not selected charged address electrodes in accordance with desired information to be entered into the display panel; and

means for applying a high level pulse of opposite polarity to a respective address electrode of the other said X or Y dimension array after [a high level of one polarity has been selected at said address electrode of said one X or Y dimension array]said selective discharging for entering the desired information into the display panel.--

18 17

--33. (Amended) A display panel according to claim 32, including means for enabling controllable discharging of said address electrode from said high level [to said low level]of said one polarity after entering said desired information into the display panel.--

19

--~~34~~. (Amended) An ac plasma panel comprising:

an array of X dimension electrodes;

an intersecting array of Y dimension electrodes with the intersections between respective X and Y electrodes defining a gas discharge cell;

address means for applying a signal to selected X and Y electrodes to discharge at least one gas discharge cell;

said address means including, means for charging [an]more than one address electrode of said X or Y dimension array to a high level of one polarity;

means for [selecting whether]selective discharging non-selected but not selected charged address electrodes to maintain the high level of one polarity at said selected charged address electrodes [or to bring the electrode to a low level of said one polarity]in accordance with desired information to be entered into the plasma panel; and

cont. C1

means for applying a high level pulse of opposite polarity to a respective address electrode of the other said X or Y dimension array after [a high level of one polarity has been selected at said address electrode of said one X or Y dimension array]said selective discharging for discharging said one gas discharge cell and entering the desired information into the plasma panel.--

20

19 --~~35~~. (Amended) An ac plasma panel according to claim ~~34~~, including means for enabling controllable discharging of said selected charged address electrodes from said high level to [said]a low level of said one polarity after entering said desired information into the plasma panel.

21
~~36~~. In display panels having panel electrodes and corresponding panel capacitance, an energy efficient method of driving said display panels through an inductor coupled to the panel electrodes comprising the steps of:

charging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

discharging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero.

22 21
~~37~~. The method of claim ~~36~~, wherein charging of the panel capacitance includes applying a forcing voltage which is about one-half the magnitude of the voltage level the panel capacitance reaches after charging.

B 1 cont

23 22
~~38~~. The method of claim ~~37~~, wherein discharging of the panel capacitance includes applying a forcing voltage which is about one-half the magnitude of the voltage level the panel capacitance reaches after charging

24 21
~~39~~. The method of claim ~~36~~, including the step of after discharging the panel capacitance, maintaining the panel capacitance in a discharged state prior to again charging the panel capacitance.

25 21
~~40~~. The method of claim ~~35~~, including the steps of after charging the panel capacitance, maintaining the panel capacitance in a charged state prior to discharge, and after discharge, maintaining the panel capacitance in a discharged state prior to again charging the panel capacitance.

26 25
~~41~~. The method of claim ~~40~~, wherein the step of maintaining the panel capacitance in a charged state includes clamping the voltage level of the panel capacitance upon the inductor current reaching zero, and wherein the step of maintaining the panel capacitance in a discharged state prior to again charging includes clamping the voltage level of the panel capacitance upon the inductor current reaching zero.

27
~~42~~. A display panel having panel electrodes and panel capacitance, an inductor coupled to the panel electrodes, and a driver circuit coupled to the inductor for operating the display panel through the inductor, the driver circuit including,

B' cont.

means for charging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

means for discharging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero.

28 27
~~43~~. A display panel according to claim ~~42~~, wherein said means for charging the panel capacitance includes means for applying a forcing voltage which is about one-half the magnitude of the voltage level the panel capacitance reaches after charging.

29 28
~~44~~. A display panel according to claim ~~43~~, wherein said means for discharging the panel capacitance includes means for applying a forcing voltage which is about one-half the magnitude of the voltage level the panel capacitance reaches after charging.

30 27
~~45~~. A display panel according to claim ~~42~~, including means for maintaining the panel capacitance in a discharged state upon the inductor current reaching zero and prior to again charging the panel capacitance.

B' cont'd

31 27
~~46~~. A display panel according to claim ~~42~~, including means for maintaining the panel capacitance in a charged state after charging the panel capacitance and prior to discharge, and means for maintaining the panel capacitance in a discharged state after discharge and prior to again charging the panel capacitance.

32
47. A display panel according to claim 46, 31 wherein said means for maintaining the panel capacitance in a charged state includes means for charging the voltage level of the panel capacitance upon the inductor current reaching zero during charging of the panel capacitance, and wherein said means for maintaining the panel capacitance in a discharged state includes means for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during discharging of the panel capacitance.

33
48. A display panel having panel electrodes and panel capacitance, and an energy recovery sustain circuit coupled to the panel electrodes for driving said display panel, said energy recovery sustain circuit including;

B cont

an inductor coupled to said panel electrodes for charging and discharging the panel capacitance;

means for charging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero;

first means for clamping the voltage level of said panel capacitance upon the inductor current reaching zero during charging of the panel capacitance;

means for discharging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

second means for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during discharging of the panel capacitance.

34 33

49. A display panel according to claim 48, wherein said first and second means for clamping includes means responsive to the inductor current reaching zero to provide said clamping independent of variations in the values of said inductor or said panel capacitance.

35

50. An energy efficient driver circuit for driving display panels having panel electrodes and panel capacitance, said driver circuit comprising:

an inductor coupled to said panel electrodes for charging and discharging the panel capacitance;

means for charging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

means for discharging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero.

3' cont

36

~~51~~. An energy efficient sustainer circuit for driving display panels having panel electrodes and panel capacitance, said sustainer circuit comprising

an inductor coupled to said panel electrodes for charging and discharging the panel capacitance;

means for charging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

first means for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during charging of the panel capacitance;

means for discharging the panel capacitance through said inductor, initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

second means for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during discharging of the panel capacitance.

3' cont.

37

~~52~~. An energy efficient sustainer circuit according to claim 36, wherein said first and second means for clamping includes means responsive to the inductor current reaching zero to provide said clamping independent of variations in the values of said inductor or said panel capacitance.

38
53. An energy efficient driver circuit for driving display panels having panel electrodes and panel capacitance, said driver circuit comprising:

an inductor coupled to said panel electrodes for charging and discharging said panel capacitance respectively to and from a desired voltage level magnitude;

first switch means coupled to said inductor to enable said panel capacitance to charge through said inductor from a first voltage level (a) initially to an intermediate voltage level magnitude which is about one-half the desired voltage level magnitude, while storing energy in said inductor, and (b) then to said desired voltage level magnitude, while removing said stored energy from said inductor; and

B' cont.

second switch means coupled to said inductor to enable said panel capacitance to discharge through said inductor from said desired voltage level magnitude (a) initially to an intermediate voltage level magnitude which is about one-half the desired voltage level magnitude, while storing energy in said inductor, and (b) then to said first voltage level magnitude, while removing said stored energy from said inductor.

39 38
54. An energy efficient driver according to claim 53, including third switch means coupled to said inductor for clamping the panel capacitance voltage level to maintain a panel capacitance discharged state until the panel capacitance is again charged.

40 38
~~55.~~ An energy efficient driver according to claim ~~52~~, including third switch means coupled to said inductor clamping the panel capacitance voltage to said desired voltage level magnitude after charging of said panel capacitance, and fourth switch means coupled to said inductor for clamping the panel capacitance voltage to said first voltage level magnitude after discharging of said panel capacitance.

B' cont.

41 40
~~56.~~ An energy efficient driver according to claim ~~55~~, wherein said third switch means and said fourth switch means each respectively includes means responsive to the end of the removal of said stored energy from said inductor to provide said respective clamping independent of variations in the value of said inductor or said panel capacitance.